

SHEET INDEX		
CONTENTS	SHEET NO.	SHEET ISSUE
SHEET INDEX		
SYMBOL		
SUPPORTING INFORMATION		
NOTES	1	2
USED-ON TABLE		
CURRENT DRAIN		
RECORD OF CHANGES		
CIRCUIT SCHEMATIC	2	1
COMPONENT LIST		
CIRCUIT DESCRIPTION	3	1


SYMBOL  
SERIAL PERIPHERAL INTERFACE  
B CIRCUIT  
ELEMENT IDENT  
A

CLER.	MOD	FUNCT	T-ERN	LOC
G061	I	009	262	262
I	009	1	102	241
I	009	2	203	242
I	009	3	301	246
I9001	I	117	243	243
I9021	I	017	2C9	2C9
I9027	U	018	2C9	2C9
I9031	U	118	2C9	2C9
I9041	I	013	2C9	2C9
I9042	I	1-3	2C9	2C9
I9F 000	I	211	248	248
I9F 010	I	314	248	248
I9F 020	U	211	248	248
I9F 031	I	310	248	248
I9F 041	I	116	247	247
I9F 050	I	214	247	247
I9F 060	I	205	246	246
I9F 070	I	304	246	246
I9F 080	I	206	246	246
I9F 090	I	305	246	246
I9F 100	I	010	246	246
I9F 110	I	109	245	245
I9F 120	I	207	245	245
I9F 130	I	307	245	245
I9F 140	I	312	242	242
I9F 155	I	212	242	242
I9F 160	P	000, 119	240	240
I9F 170	P	000, 119	240	240

DIG ISS	PREV FUND	STD	IMP DISC	SCL NOTL

SYSTEM USED ON	DESIGN CONTROL
COMMON SYSTEMS	IH

NOTES:

1.  GROUND RETURN
2. UNLESS OTHERWISE SPECIFIED:  
RESISTANCE VALUES ARE IN OHMS  
CAPACITANCE VALUES ARE IN MICROFARADS  
VALUES PRECEDED BY THE SYMBOL +(PLUS)  
OR -(MINUS) ARE IN VOLTS

- ### 3. BATTERY AND GROUND TERMINALS FOR INTEGRATED CIRCUITS

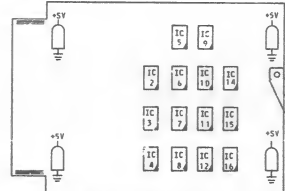
[illegible]

4. BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT PACK ARE AS FOLLOWS:

FUNCTION	TERMINAL
+5	000,119
GND	200,319

5. HORIZONTAL MOUNTING CENTERS AT 0.50 INCH.

6. INTEGRATED CIRCUIT LOCATION GUIDE:
- 
- (COMPONENT SIDE SHOWN)



UNMARKED COMPONENTS ARE FILTER CAPACITORS

## SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT PACK CODE	JK9
CONNECTOR ON FRAME	947C OR 947A
SERIES FOR LATEST CLASS A CHANGE (ANY HIGHER SERIES IS ACCEPTABLE)	
ACCEPTABLE SERIES	1

SHEET INDEX NOTES

1. WHEN CHANGES ARE MADE IN THIS DRAWING ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.
2. THIS SHEET INDEX WILL BE REISSUED AND BROUGHT UP TO DATE EACH TIME ANY SHEET OF THE DRAWING IS REISSUED, OR A NEW SHEET IS ADDED.
3. THE ISSUE NUMBER ASSIGNED TO A CHANGED OR NEW SHEET WILL BE THE SAME ISSUE NUMBER AS THAT OF THE FIRST SHEET.
4. SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NUMBER.
5. THE LAST ISSUE NUMBER OF THE FIRST SHEET INDEX IS RECOGNIZED AS THE LATEST ISSUE NUMBER OF THE DRAWING AS A WHOLE.

**NOTICE-** NOT FOR USE OR DISCLOSURE OUTSIDE THE BELL SYSTEM EXCEPT UNDER WRITTEN AGREEMENT.

JK9 CIRCUIT PACK

### BUS TERMINATION CIRCUIT

1198

AT&T  
STANDARD

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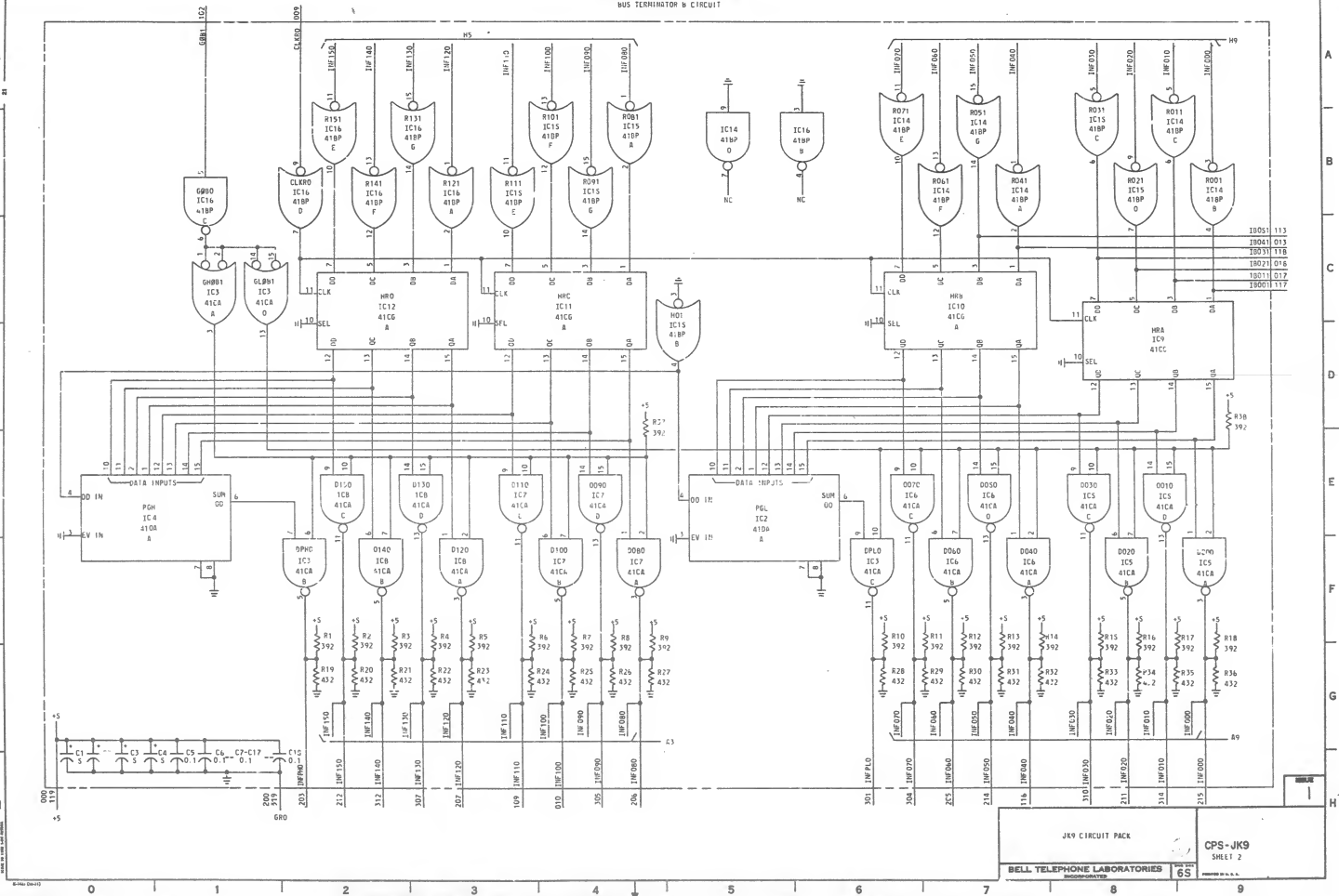
CPS- JK9  
3 SHEETS

BELL TELEPHONE LABORATORIES  
INCORPORATED

# PART OF CPS JK9

NUS TERMINATOR IN CIRCUIT

6X1-5C3



JK9 CIRCUIT PACK

BELL TELEPHONE LABORATORIES

INCORPORATED

CPS-JK9

SHEET 2

60

REPRODUCED IN U.S.A.

# PART OF CPS JK9

BUS TERMINATOR 3

## COMPONENT LIST INTEGRATED CIRCUIT

LOC CODE ELIM	IC2 410A		IC3 41CA		IC4 41DA		IC5 41CA		IC6 41CA		IC7 41CA		IC8 41CA	
ID	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A	PGL	2E5	GHB01	2C1	FGH	2E1	000	2F9	0040	2F7	0080	2F4	0120	2F3
B			0PMD	2F2			0020	2F8	0060	2F7	0100	2F4	0160	2F2
C			0PLD	2F4			0030	2E8	0070	2E6	0110	2E3	0150	2F2
D			GJBB1	2C1			0010	2E8	0050	2E7	0090	2F4	0130	2F3
E														
F														

LOC CODE ELIM	IC9 41CG		IC10 41CG		IC11 41CG		IC12 41CG		IC14 41BP		IC14 41BP			
ID	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC		
A	HRA	2C8	HBB		HRC	2C4	HBD	2C2	RD41	287	RD81	284	R121	283
B									RD21	289	RD1	285	SPARE	284
C									R111	288	RD31	288	CBIO	281
D									SE30E	285	RD21	288	CLRD	282
E									RD71	286	R111	283	R151	282
F									RD61	287	R101	284	R141	287
G									RD51	287	RD91	284	R131	283

## CAPACITOR

DESIG	CODE
C1-C4	601A, 5
C5-C18	KS-19774 L5, D.1

## RESISTOR

DESIG	CODE
R1-R18	KS-20616 L10, 392
R19-R36	KS-20616 L10, 432
R37	KS-20616 L10, 392
R38	KS-20616 L10, 392

## CIRCUIT DESCRIPTION

### BUS TERMINATOR B CIRCUIT

THIS CIRCUIT PACK CONTAINS A 16 BIT HOLDING REGISTER. THE 16 OUTPUTS OF THE REGISTER FEED INTO TWO 8-BIT PARITY TREES. THE OUTPUT OF EACH OF THE PARITY TREES IS A ONE WHENEVER THERE ARE AN ODD NUMBER OF ONES PRESENT AT THE INPUTS. THE STATES OF THE 16 INFORMATION LEADS J10500 J10150 ARE CLERED INTO THE HOLDING REGISTER AT THE TRAILING EDGE OF A GROUND GOING PULSE AND CLKLINE. CLKRD. THE CONTENTS OF THE REGISTER AND THE ASSOCIATED PARITY BITS CAN BE GATED INTO THE INFORMATION LEADS BY SETTING LEAD 0001 TO A LOGICAL ONE.

TRANSMISSION LINE TERMINATIONS ARE PROVIDED BY THE RESISTIVE VOLTAGE DIVIDERS FOR EACH OF THE 16 INFORMATION BUS LEADS. THE 41CA'S ARE OPEN COLLECTOR BUS DRIVERS. THE 4 LEAST SIGNIFICANT BITS OF THE INFORMATION LEADS ARE INVERTED AND CONNECT TO JK9 FOR THE PURPOSE OF DEVICE DECODING.

JK9 CIRCUIT PACK

BELL TELEPHONE LABORATORIES  
PHILADELPHIA, PA.

CPS-JK9  
SHEET 3

65